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Deep Submicron Signal Integrity and Testing

by

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Outline

First question:

How does scaling in deep submicron effect the quality of signals?

Answer:

By signal propagation effects on interconnects

➜ What are the (significant) effects?

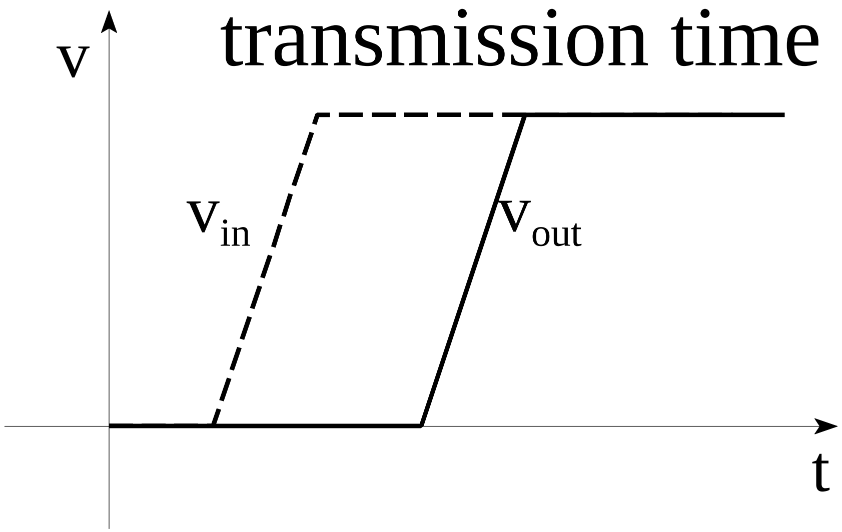
➜ How can we model these effects?

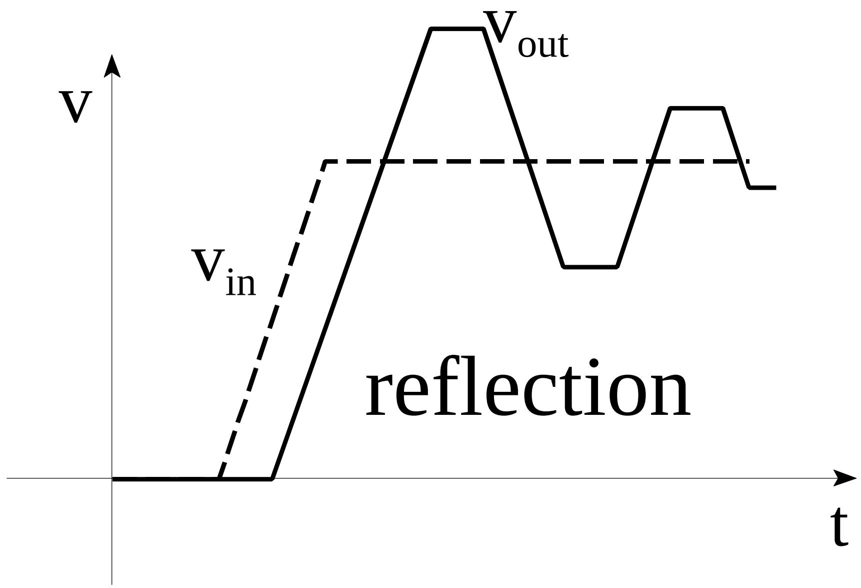
Second question:

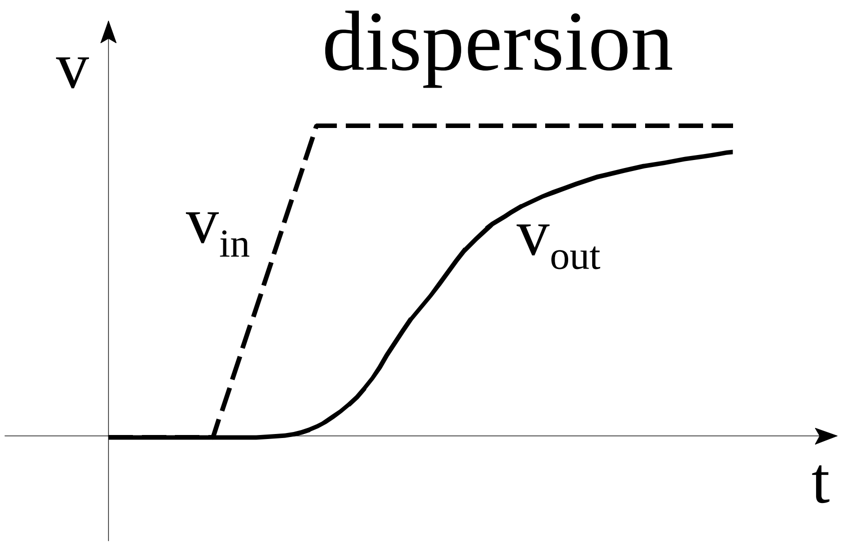
What is the impact on testing?

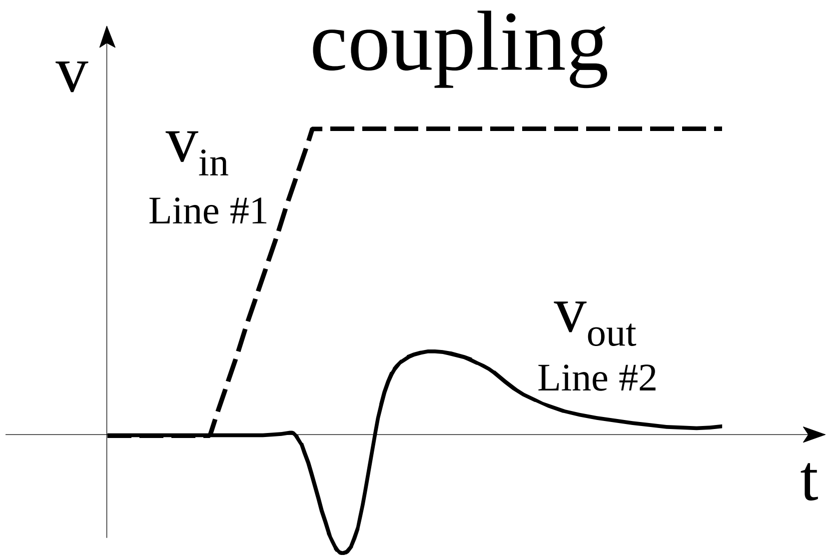
Outline

Significant effects:

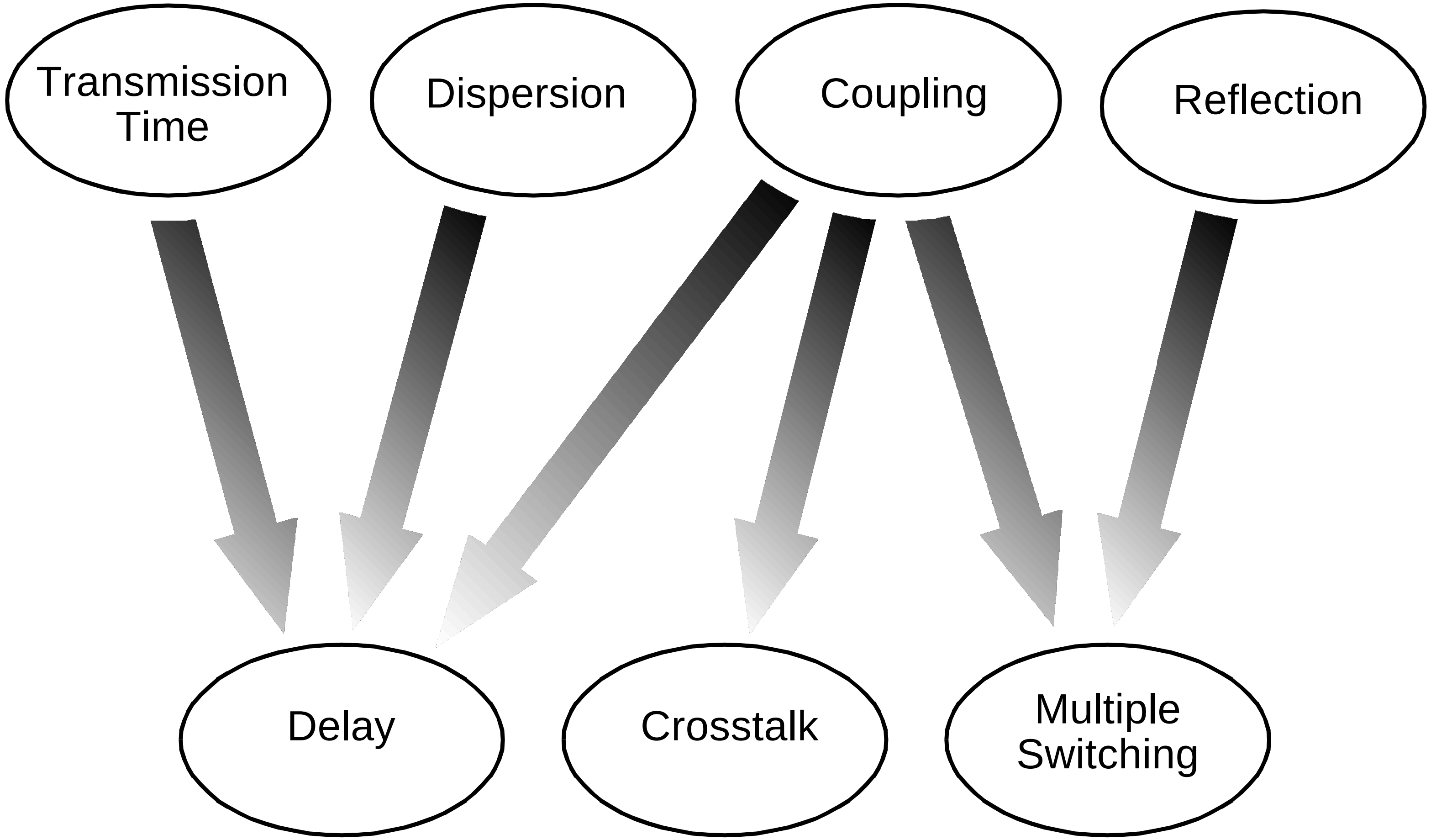








Results from interconnect effects on (digital) circuits



Question:

How can we model these effects?

Answer:

Using Maxwell's Equations

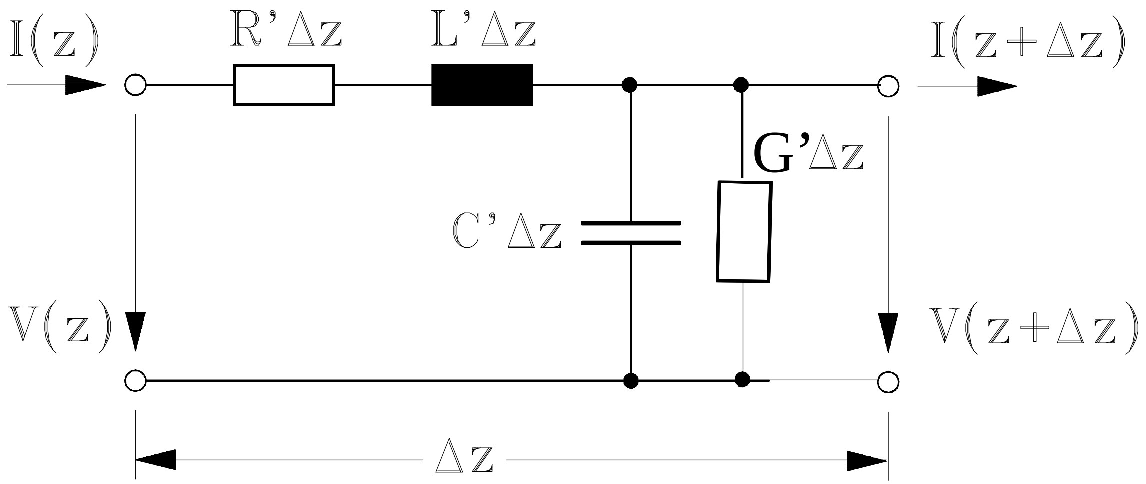
➜ Telegraphers Equations:

$$\frac{\partial \underline{v}(z,t)}{\partial z} = -\left(\mathbf{R} \quad \mathbf{L}\ \frac{\partial}{\partial t} \right) \underline{i}(z,t)$$

$$\frac{\partial \underline{i}(z,t)}{\partial z} = -\left(\mathbf{G} \quad \mathbf{C}\ \frac{\partial}{\partial t} \right) \underline{v}(z,t)$$

Types of modeling

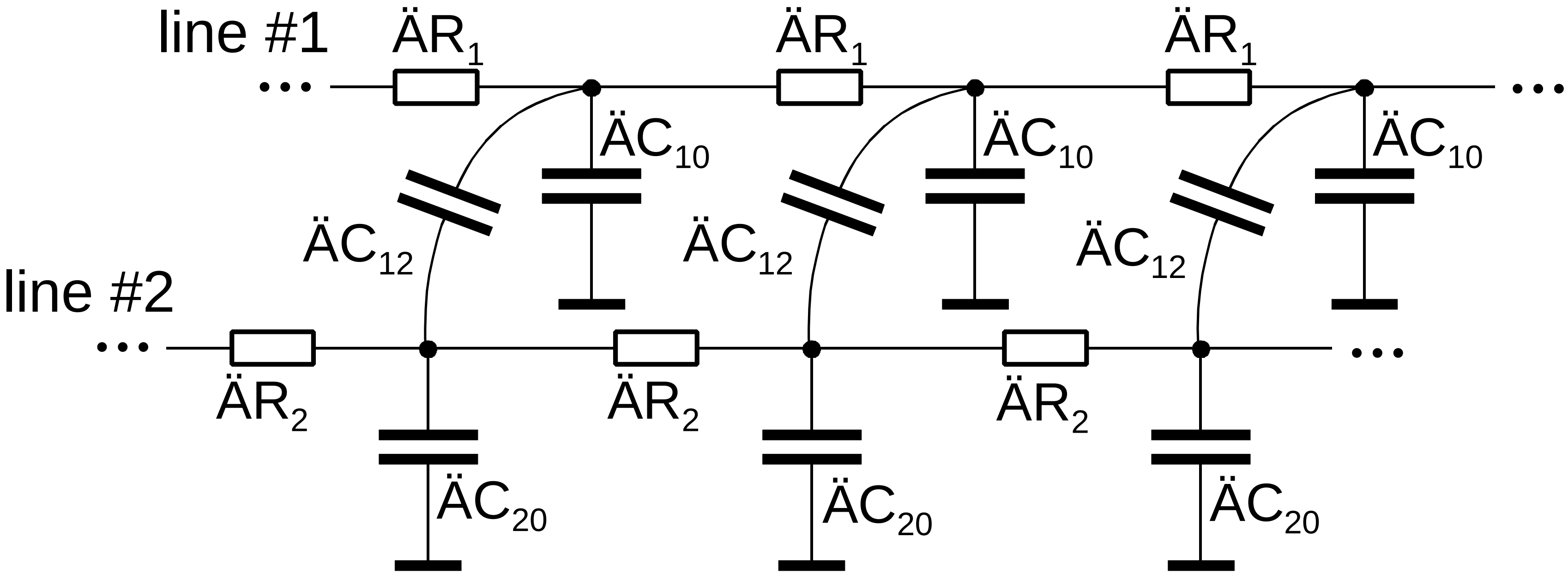
1. Lumped element model (commonly used):



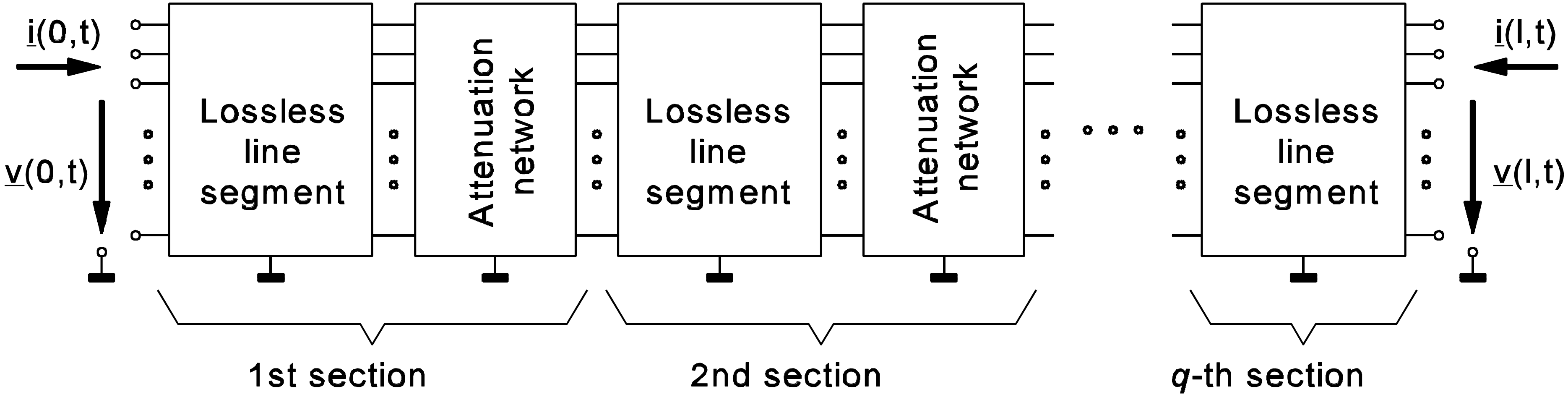
advantage: simple for use in general purpose network analysis programs

disadvantage: strictly speaking: wrong

State of practice: modeling of line systems



2. Distributed model; e.g. WIRE:



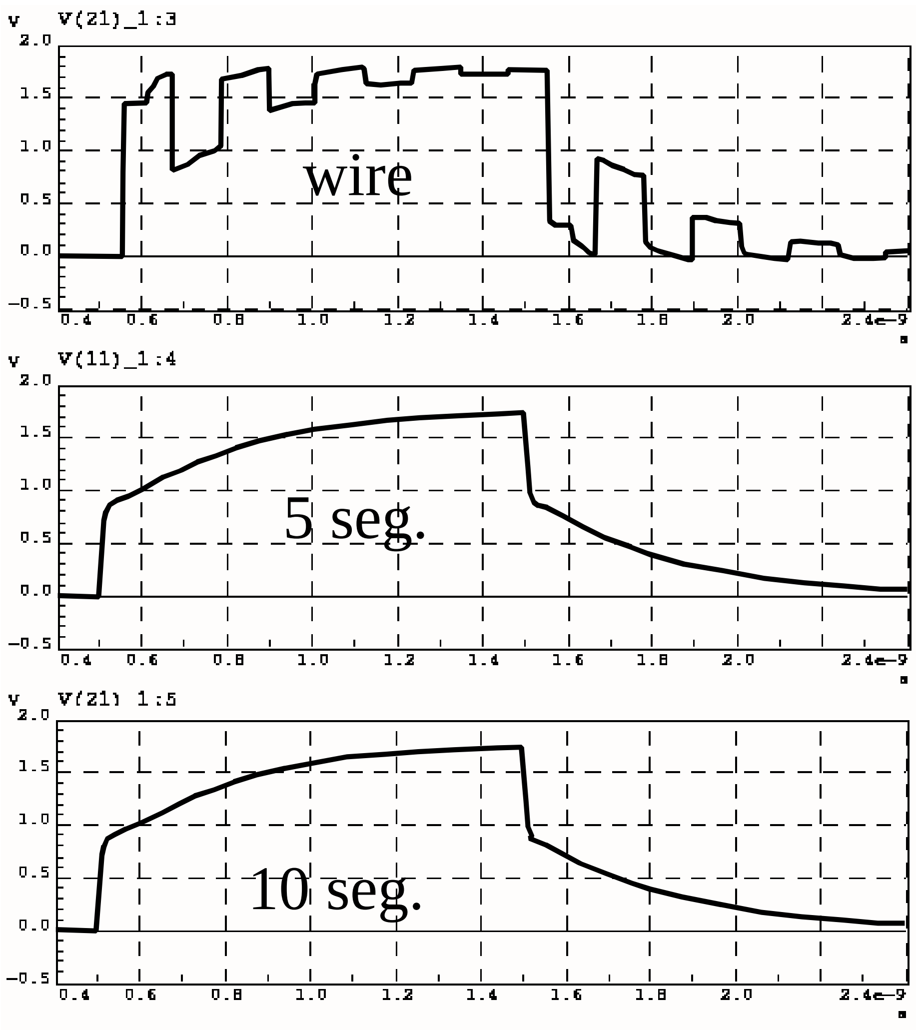
Solution:

$$\underline{v}_1^k(t) = \left(\mathbf{1} - \mathbf{A}_1^k\right) \otimes \underline{v}_2^k\left(\mathbf{1}t - \mathbf{T}^k\right) \quad \mathbf{A}_2^{k-1} \otimes \underline{v}_1^{k-1}\left(\mathbf{1}t - \mathbf{T}^k\right)$$

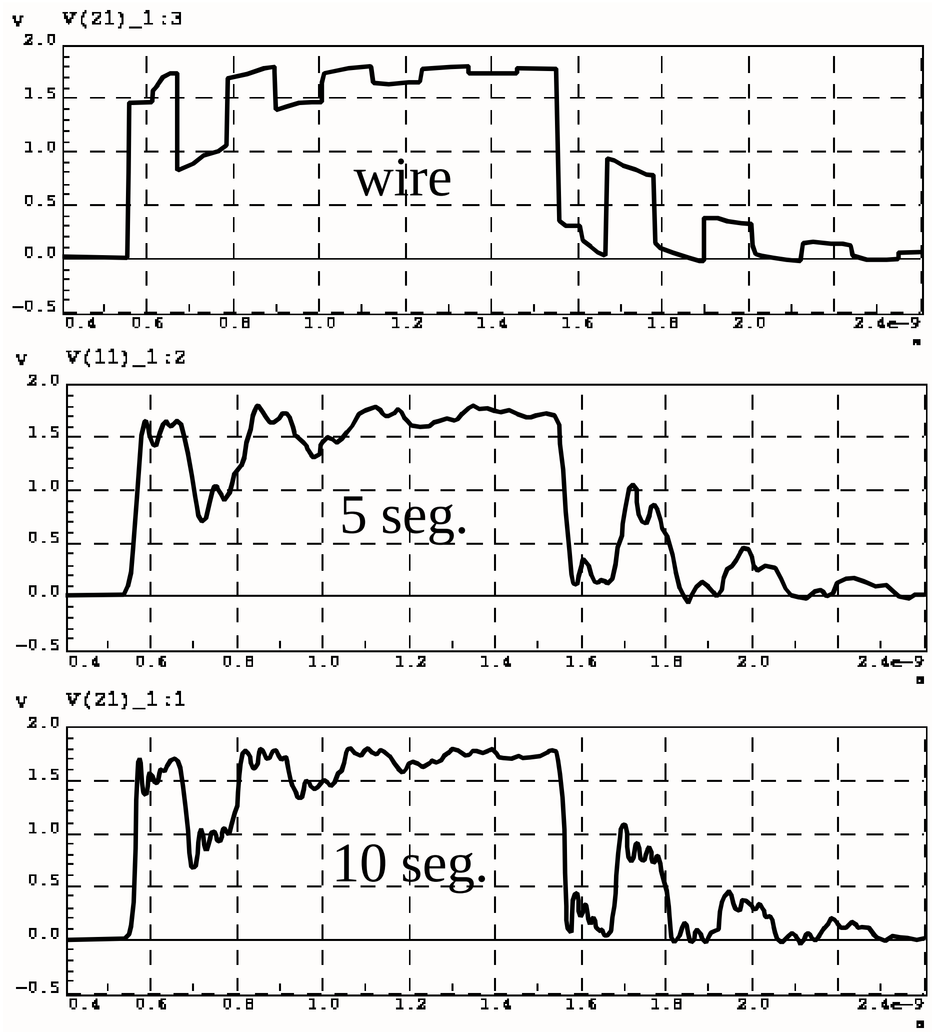
$$\underline{v}_2^k(t) = \left(\mathbf{1} - \mathbf{A}_1^k\right) \otimes \underline{v}_1^k\left(\mathbf{1}t - \mathbf{T}^k\right) \quad \mathbf{A}_2^{k\ \ 1} \otimes \underline{v}_2^{k\ \ 1}\left(\mathbf{1}t - \mathbf{T}^k\right)$$

Examples for medium losses: comparison

wire - rlc

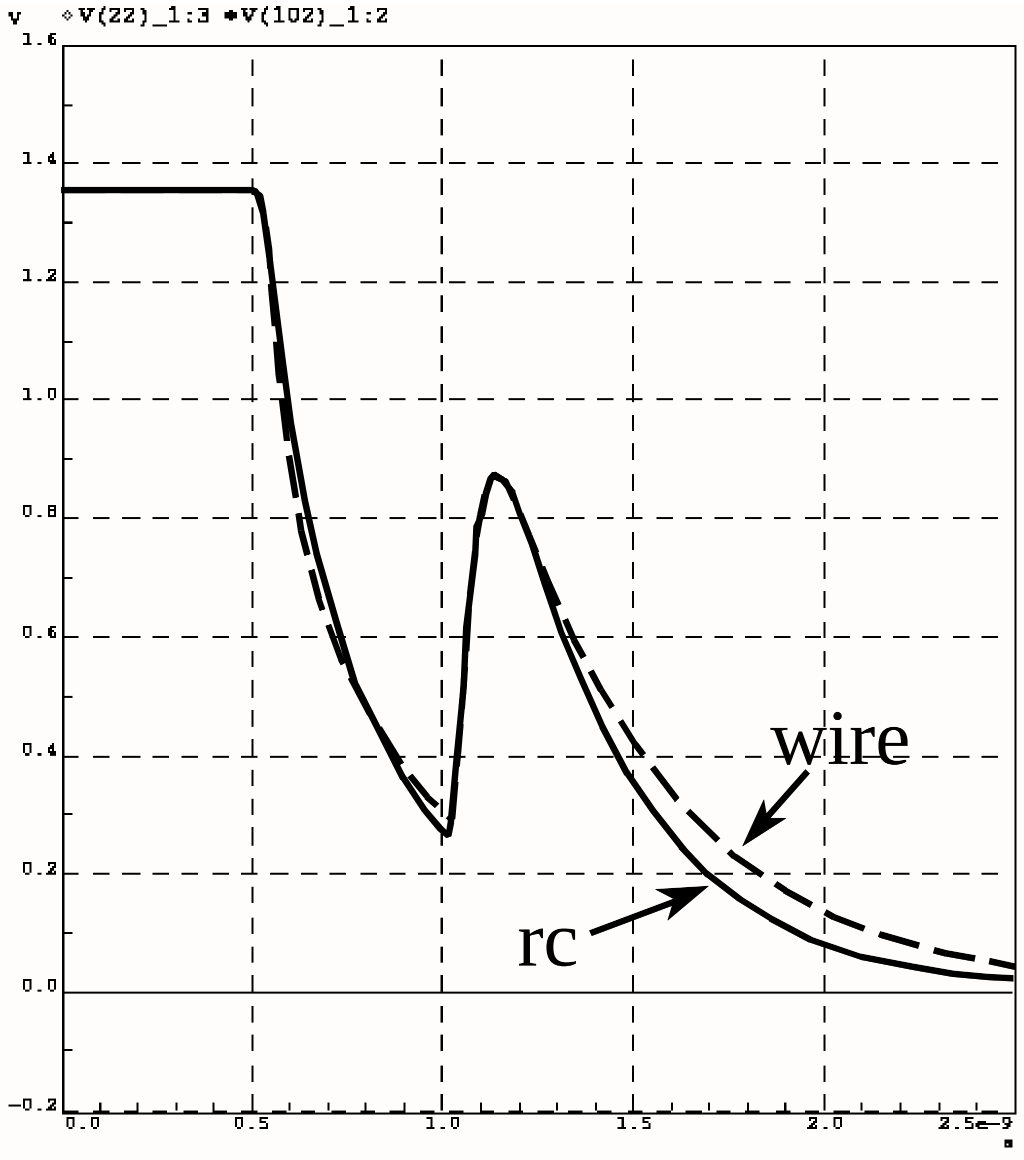


wire - rc



2-line system, 0.18µ, M5, output driven line, R’ = 8 kÙ/m

Example for high losses: comparison wire - rc



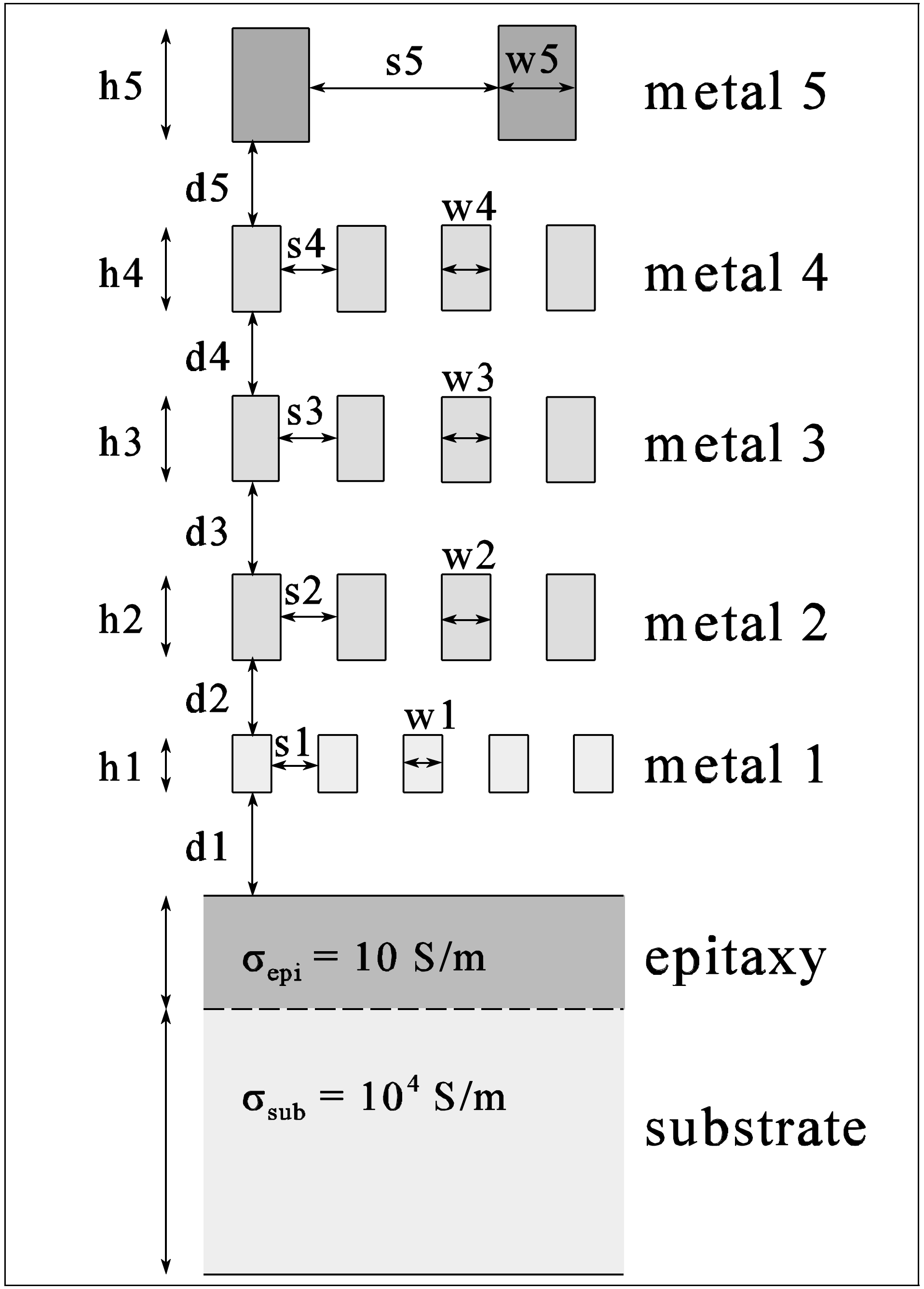
9-line sytem, 0.13µ, M5, oddmode, centre line, rc: 10 segments

Outline

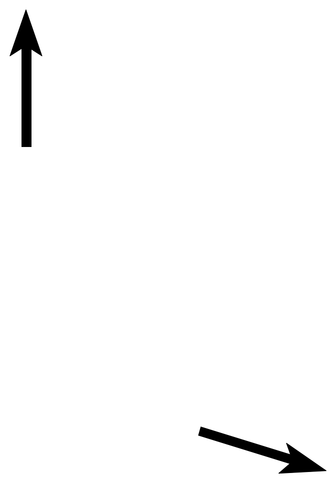
Question:

Have interconnects to be taken into account for testing?

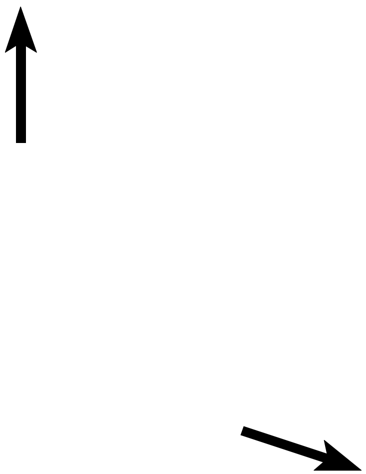
Data (in μm) obtained from SIA-Roadmap					
technology	**0.35μ**	**0.25μ**	**0.18μ**	**0.13μ**	**0.1μ**
w1	≥0.4	≥0.3	≥0.22	≥0.15	≥0.11
w2, w3, w4	≥0.6	≥0.45	≥0.33	≥0.22	≥0.16
w5	≥0.8	≥0.6	≥0.44	≥0.3	≥0.22
s1	≥0.5	≥0.35	≥0.25	≥0.18	≥0.13
s2, s3, s4	≥0.6	≥0.45	≥0.33	≥0.22	≥0.16
s5	≥2.0	≥1.5	≥1.1	≥0.75	≥0.55
h1	0.6	0.6	0.55	0.45	0.38
h2, h3, h4	0.9	0.9	0.82	0.66	0.56
h5	1.2	1.2	1.1	0.9	0.77
d1	1.0	1.0	0.9	0.75	0.75
d2, d3, d4, d5	0.9	0.9	0.8	0.7	0.7
epitaxy	3.0	2.0	1.4	1.0	0.8
substrate	400	400	400	400	400
signal rise time	150ps	100ps	75ps	55ps	45ps
V_{DD}	3.3V	2.5V	1.5V	1.35V	1.2V



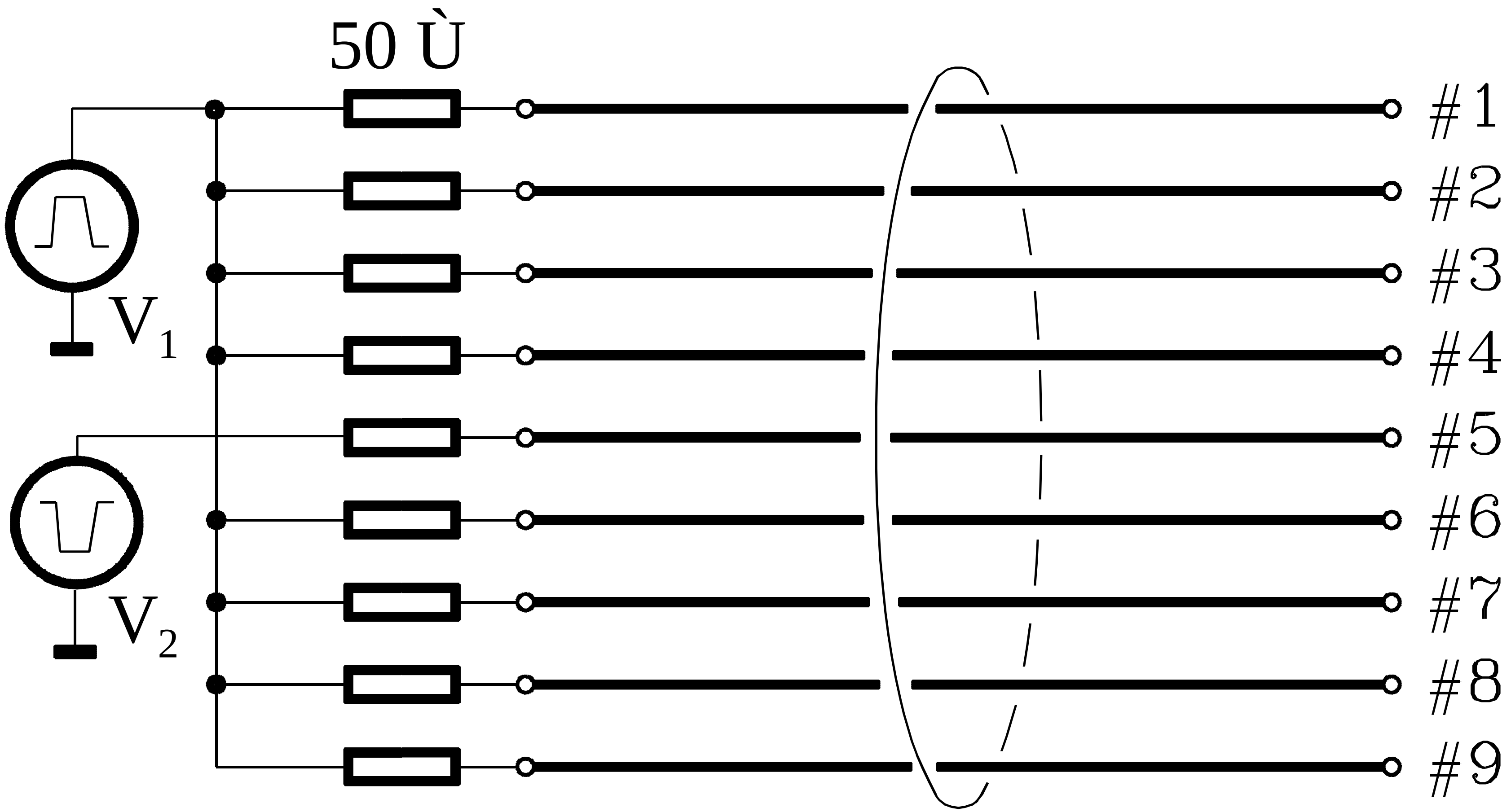
Capacitances to ground (C'_{10})



Coupling capacitances (C'_{12}) vs. technology

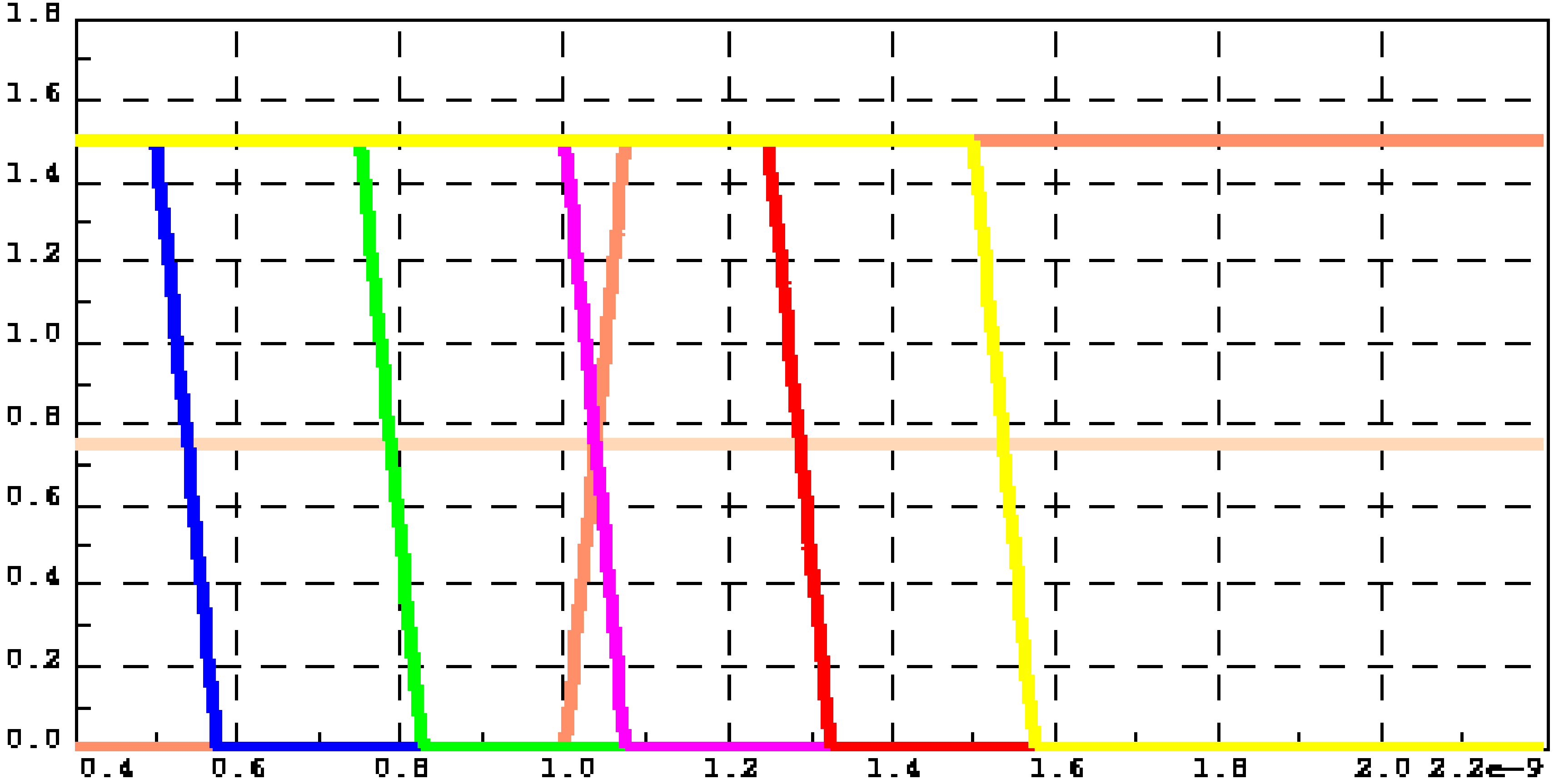


Example: Interconnect system



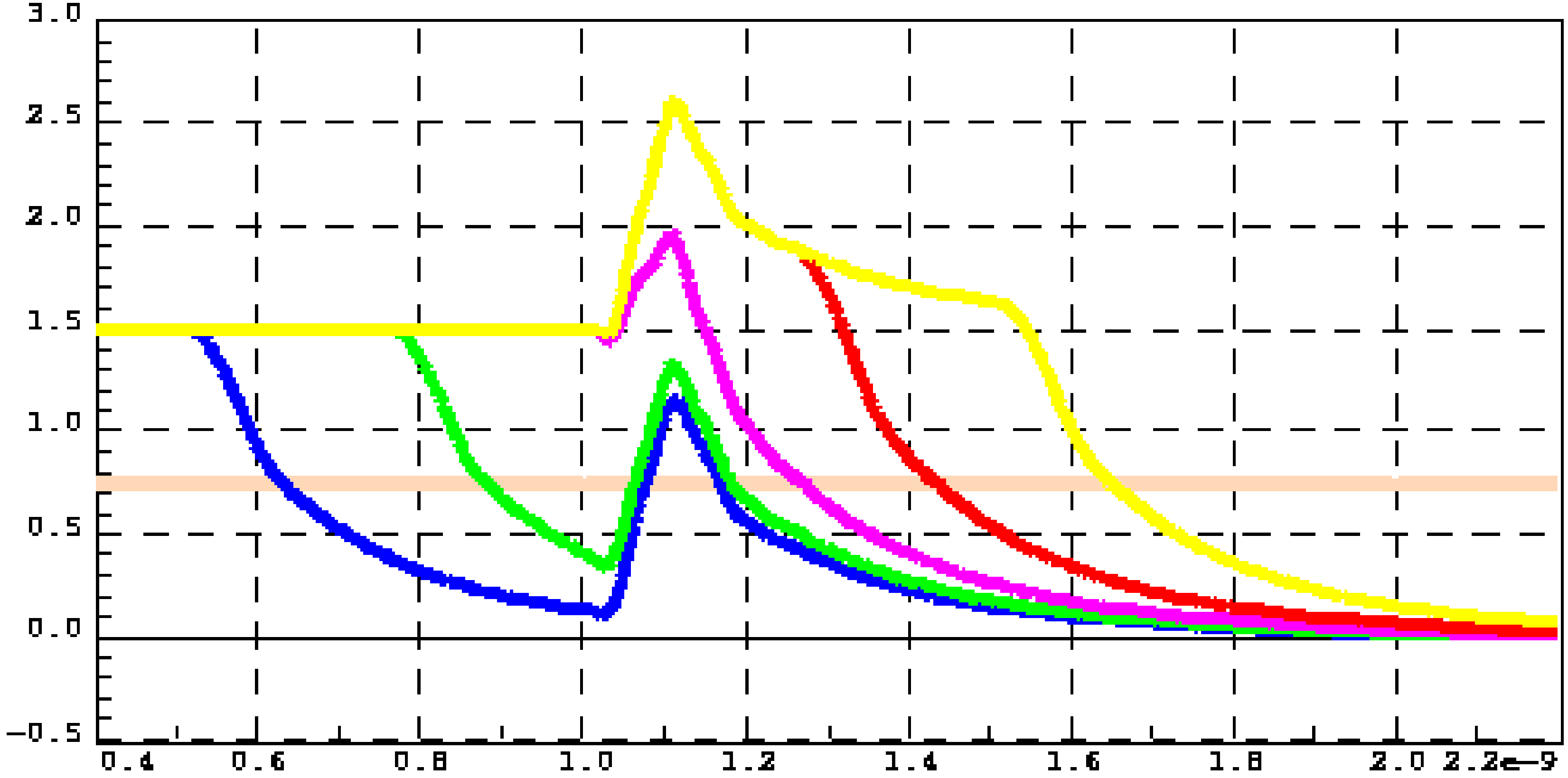
Occurence of additional delays and hazards due to coupling effects on interconnects

Input signals:



Occurence of additional delays and hazards due to coupling effects on interconnects

Output signals:



Delay and hazards vs. technology: Metal 1

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Outline

1 Introduction

2 Modeling of interconnects

3 Impact on testing

4 Summary

Summary and conclusion

1. For high losses: interconnects can be modeled using rc-elements with capacitive coupling to the nearest neighbouring lines.

2. For low and medium losses: interconnects have to be modeled using distributed models including inductances.

Summary and conclusion (cont.)

3. There is a strong pattern dependancy concerning the occurence of line delays and hazards.

⇨ For the test pattern generation one has to take into account effects on interconnects.